

WHAT IS CLAIMED IS:

- 1 1. Level shifting circuitry, comprising:
2 a level-shifting section responsive to an input logic signal, such input logic signal
3 having a first voltage level representative of a first logic state or a second voltage level
4 representative of a second logic state, such level-shifting section providing an output
5 logic signal at an output terminal thereof having a third voltage level representative of the
6 first logic state of the input logic signal;
7 an enable/disable section, responsive to an enable/disable signal, for placing the
8 output terminal at a relatively high output impedance condition independent of the logic
9 state of the input signal during a disable mode.
10 (In one embodiment) the level-shifting section includes an additional transistor.
11 The additional transistor has a control electrode connected to the junction, a first
12 electrode coupled to the source of the third voltage level through the first switching
13 transistor and a second electrode connected to the second electrode of the input transistor.
14 (In one embodiment) the input transistor and the additional transistor are of opposite
15 conductivity type.
- 1 2. The level shifting circuitry recited in claim 1, wherein the level-shifting section
2 includes:
3 an input transistor having a control electrode, a first electrode coupled to the input
4 logic signal, and a second electrode;
5 a first switching transistor;
6 a second switching transistor;
7 an output pair of serially coupled complementary type transistors, a first one of
8 the pair of transistors having a first electrode coupled to a source of the third voltage level
9 through the first switching transistor and a control electrode coupled to the second
10 electrode of the input transistor, a junction between the output pair of transistors
11 providing the output terminal for the level-shifting circuitry, a control electrode of the
12 second one of the pair of transistors being connected to the first electrode of the input

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13 transistor, the second one of the pair of transistors having a second electrode coupled to
14 the second voltage level through the second switching transistor; and
15 wherein the first and second switching transistors are fed by the enable/disable
16 signal.

1 3. The level-shifting circuitry recited in claim 2 wherein the enable/disable circuit
2 includes an inverter, and wherein such inverter is fed by the enable/disable signal,
3 such inverter having an output coupled to the control electrode of the first switching
4 transistor.

1 4. The level-shifting circuitry recited in claim 3 wherein the inverter is powered by a
2 source of the first voltage level.

1 5. The level shifting circuitry recited in claim 4 wherein the control electrode of the
2 input transistor is coupled to the source of the first voltage level.

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1 6. The level shifting circuitry recited in claim 4 wherein the inverter comprises:
2 a level shifter for shifting the level of the enable/disable signal from the first
3 voltage level to the third voltage level and for feeding such third voltage level to the
4 control electrode of the first switching transistor to placing the first switching transistor to
5 a non-conducting condition during the disable mode.

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